DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-28, 30-50 and 83-94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (US 5,825,449) in view of Taguchi (Taguchi et al., US 6,121,632) and/or Kwasnick (Kwasnick et al., US 5,198,694; of record) and further in view of Hayashi (US 6,094,248).

Shin discloses a semiconductor device (Figs. 1a-1f; also see col. 1, lines 34-67; a liquid crystal display device), comprising: a substrate (1; glass); a thin film transistor comprising a gate electrode (2), a first insulating layer over the gate electrode, a channel forming region in a first semiconductor layer (4), and doped source and drain regions in a second semiconductor layer (5); a second interlayer insulating layer (9; nitride, inorganic); a pixel electrode (6); a storage capacitor wiring ("20" and/or "2D"); and, a source input terminal portion (a source pad, also see the top row pads 640 in Fig. 6) including a first layer (2A) comprising the same material as that of the gate electrode (2) and a second layer (6A) comprising the same material as that of the pixel electrode in contact with the first layer through a contact hole formed only in the first insulating layer, wherein the gate electrode, the storage capacitor wiring layer and the first layer in

the input terminal portion all have a tapered portion and are formed from a same conductive layer; and the storage capacitor wiring and a portion of the pixel electrode, with a portion of the first insulating layer disposed therebetween, inherently form a storage capacitor. The device further comprises a source (or first) wiring (7; also see source wiring 610 in Fig. 6), wherein a portion of the wiring (7) is formed over the source region (left side of film 5) and another portion of the source wiring (7) is formed on the second layer (6A) of the source input terminal portion. And, it is also noted that the second insulating layer (9) in Shin can be regarded as being naturally overlapping with the pixel electrode (6), as the second insulating layer (9) therein overlaps with at least a portion of the pixel electrode (6).

Shin further discloses that the first layer (2A) of the input terminal portion directly contacts the second layer (6A) of the input terminal portion.

Shin does not expressly disclose that the channel formation region (i.e., the first portion) of the first semiconductor layer can have a thickness thinner than that of the rest of the first semiconductor layer. However, one of ordinary skill in the art would readily recognize that such thinner portion can be desirably formed through over etching of the overlying heavily doped source/drain layer (i.e., the second semiconductor layer) so as to prevent any potential shorting from happening by any residuals of the overlying heavily doped source/drain layer, as evidenced in Taguchi (see the thinner portion of the channel region in layer 12 in the cover page figure) and/or Kwasnick (see the thinner portion of the channel region in layer 30 in the cover page figure).

Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to incorporate the feature of the thinner first portion in the channel formation region, such as that taught in Taguchi and/or Kwasnick, into the device of Shin, so that a semiconductor device would be obtained with the potentially adverse electrical shorting to the channel region therein being eliminated.

Furthermore, although Shin does not expressly disclose that the gate electrode can comprise aluminum and that the pixel electrode can comprise indium, zinc and oxygen, aluminum is one of most commonly used materials for forming the gate electrode, and In-Zn-O is one of most commonly used materials for forming the pixel electrode, as readily evidenced in the prior art such as Hayashi (US 6,094,248; see col. 5, lines 43-53; and col. 7, lines 58-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time invention was made to incorporate the art-known commonly-used Al-gate electrode and Ti-Zn-O pixel electrode into the device collectively taught above, so that a semiconductor device with desired materials and/or with improved material flexibilities for the gate and pixel electrodes would be obtained, since these materials are art-known ones that are respectively well suited for the intended uses, and it has been held that:

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claims 26-28, 30 and 35-38, it is noted that the storage wiring ("20" or "2D") in Shin can be regarded as being covered by the pixel electrode (6), as at least a portion of the storage wiring is directly covered vertically by the pixel electrode, and/or the storage wiring can be fully covered by the pixel electrode when view along certain directions/angles.

Regarding claims 39-42, it is further noted that, about the selected applications as recited in these claims, each of these recited application are art-known applications for an LCD device such as the one collectively taught above, in order to achieve better display performance with reduced size, as readily evidenced in the prior art such as Ikeda et al. (US 5,428,250; see col.1, lines 16-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above semiconductor device collectively taught above, and applied it to any of the art-known applications, so that a device in any of the applications with reduced size and/or with improved display performance would be obtained.

Regarding claims 43-50, it is noted that at least a portion of the source wiring (or first wiring; 7) in Shin is covered by the second insulating layer (9) therein.

Regarding claims 83-86, it is noted that the angle of the tapered portion in Shin is substantially between 1^{o} and 20^{o}, given that the lateral and vertical dimensions shown in Figs. 1a-1f of Shin are obviously in significantly different scales, as the actual lateral dimension of the TFT therein should be normally much greater than its thickness dimension, in a manner substantially same as what is shown in Fig. 8 of the instant invention. Furthermore, it is noted that the angle of the tapered portion is an art-

recognized parameter of importance subject to routine experimentation and optimization.

Regarding claims 87-96, it is noted that it is well known in the art that micro-crystal semiconductor is also commonly used to form the channel forming layer in TFT, so as to achieve the desired material choice and/or desired combination of performance and cost for the TFT, as readily evidenced in the prior art such as Iwata (US 5,144,391; see col. 1, lines 13-20) and/or Shimizu (US 5,834,345; see its abstract).

Response to Arguments

Applicant's arguments filed on February 07, 2008 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Shin expressly discloses the claimed features, including that the first layer (2A) of the input terminal portion directly contacts the second layer (6A) of the input terminal portion. And, as evidenced in Hayashi, it is well-known in the art that aluminum is one of most commonly used materials for forming the gate electrode, and In-Zn-O is one of most commonly used materials for forming the pixel electrode. Accordingly, it would be well within the ordinary skill in the art to incorporate the art-known commonly-used Al-gate electrode and Ti-Zn-O pixel electrode into the device of

Shin, so as to make a semiconductor device with desired materials and/or with improved material flexibilities for the gate and pixel electrodes, since these materials are art-known ones that are respectively well suited for the intended uses, and it has been held that:

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

In response to applicant's argument that the claimed invention achieved improvements in heat stability and corrosion prevention with the recited materials for the gate electrode and pixel electrode, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). And, same improvement would be naturally achieved in the above collectively taught device since it would be formed with a structure and/or a material set that are each substantially same as that of the instant invention.

Applicant's other arguments with respect to the above rejected claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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/Shouxiang Hu/
Primary Examiner, Art Unit 2811